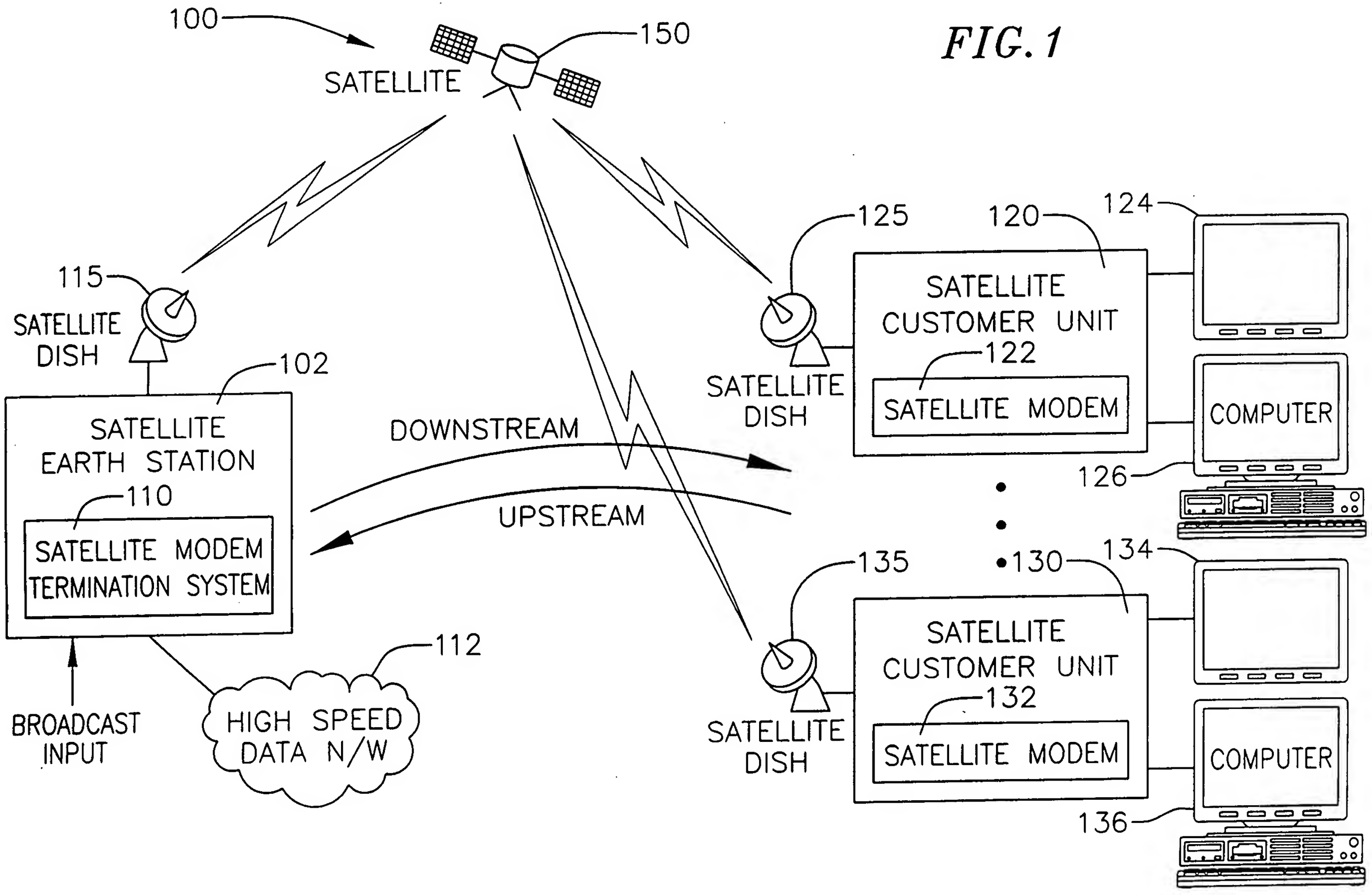

100
SATELLITE
150
115
SATELLITE
DISH
102
SATELLITE
EARTH STATION
110
SATELLITE MODEM
TERMINATION SYSTEM
BROADCAST
INPUT
112
HIGH SPEED
DATA N/W
DOWNSTREAM
UPSTREAM
125
SATELLITE
DISH
120
SATELLITE
CUSTOMER UNIT
122
SATELLITE MODEM
124
COMPUTER
126
135
SATELLITE
DISH
130
134
SATELLITE
CUSTOMER UNIT
132
SATELLITE MODEM
COMPUTER
136

FIG. 1

FIG.2

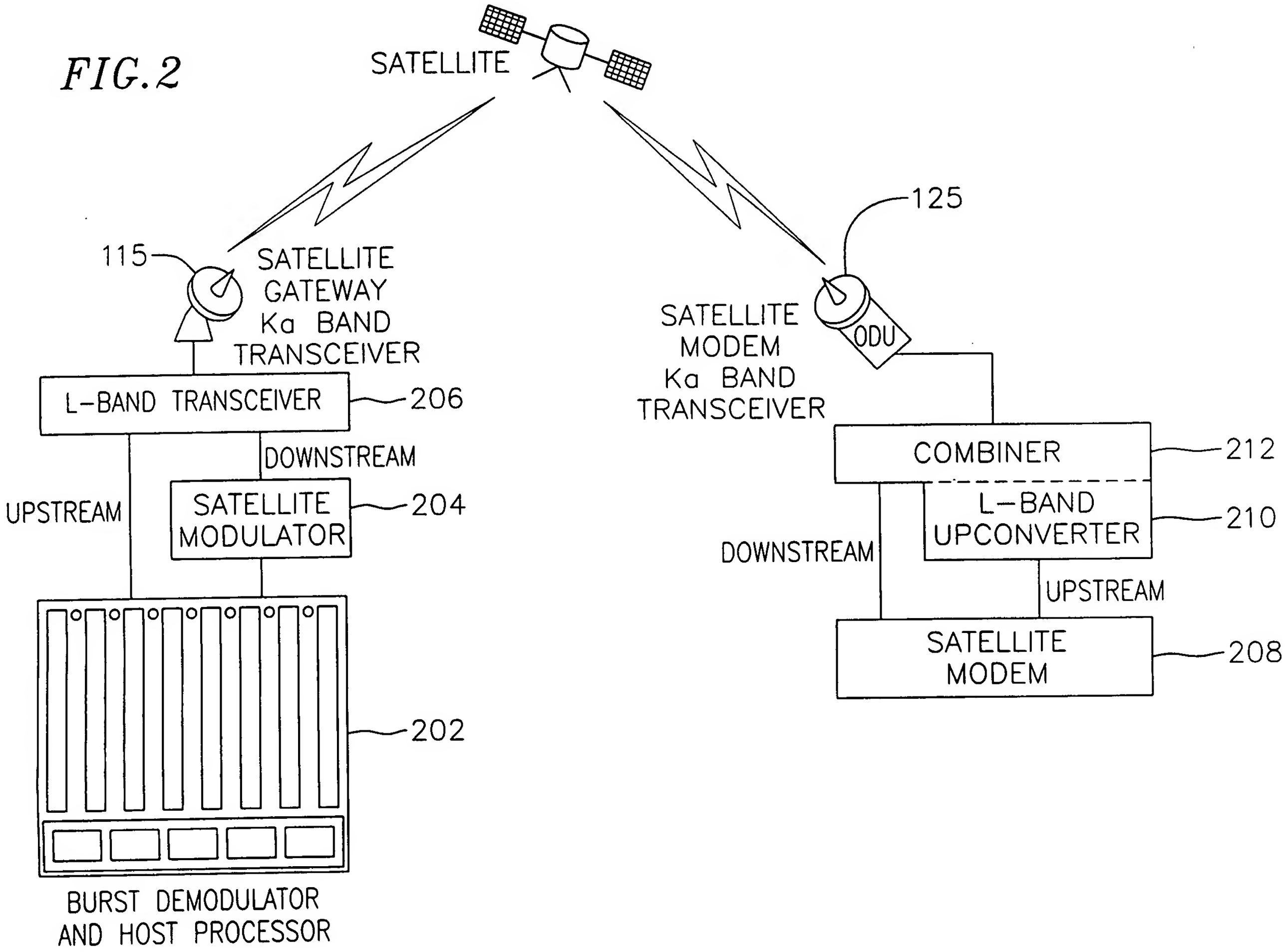

SATELLITE
115
SATELLITE GATEWAY Ka BAND TRANSCEIVER
L-BAND TRANSCEIVER
206
DOWNSTREAM
UPSTREAM
SATELLITE MODULATOR
204
202
BURST DEMODULATOR AND HOST PROCESSOR
125
SATELLITE MODEM Ka BAND TRANSCEIVER
ODU
COMBINER
212
L-BAND UPCONVERTER
210
DOWNSTREAM
UPSTREAM
SATELLITE MODEM
208

FIG.3

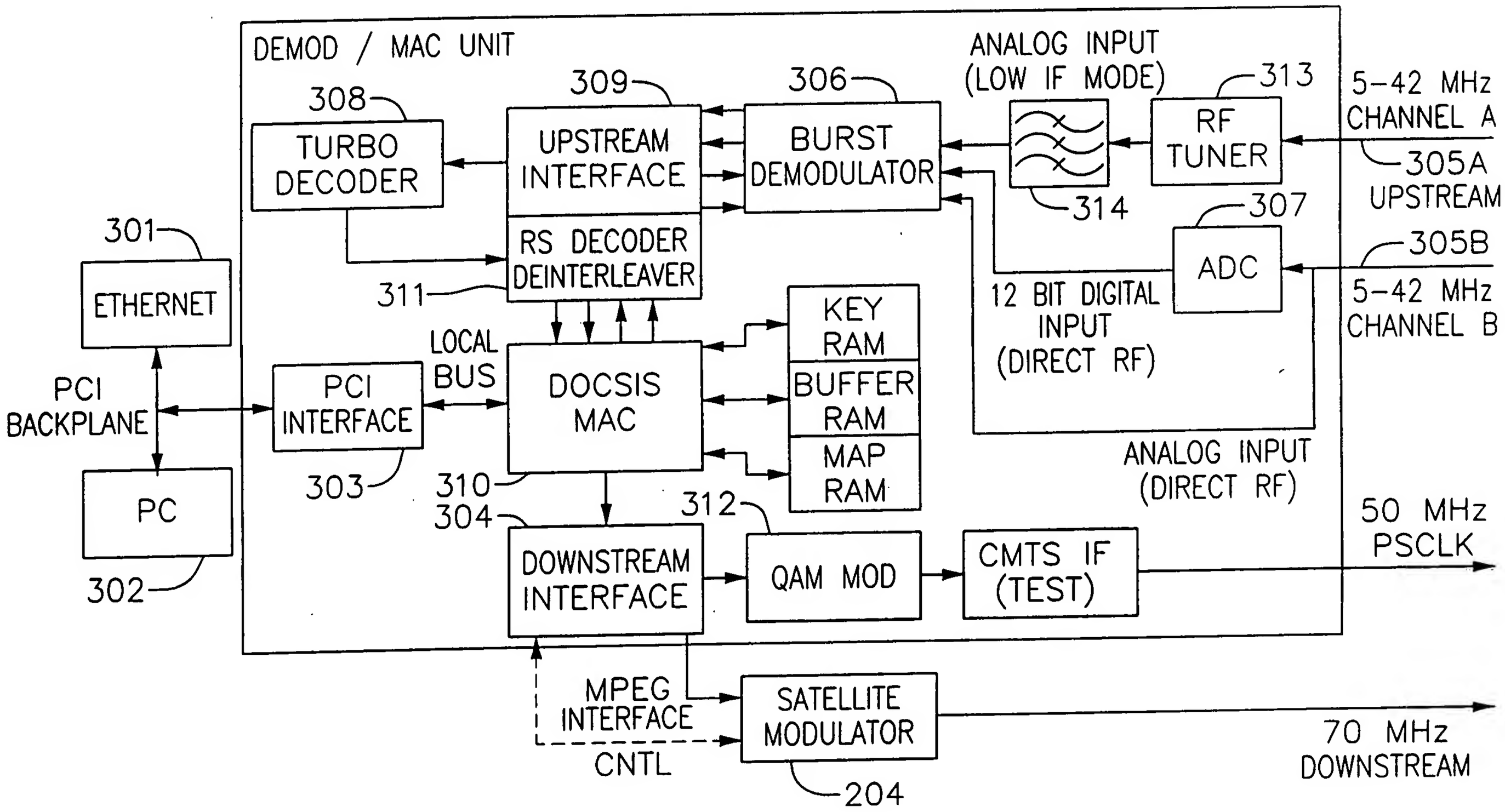

DEMOD / MAC UNIT
308
TURBO DECODER
309
UPSTREAM INTERFACE
306
BURST DEMODULATOR
ANALOG INPUT (LOW IF MODE)
313
RF TUNER
5-42 MHz CHANNEL A
305A
UPSTREAM
314
307
ADC
305B
5-42 MHz CHANNEL B
301
ETHERNET
RS DECODER DEINTERLEAVER
311
LOCAL BUS
KEY RAM
BUFFER RAM
MAP RAM
12 BIT DIGITAL INPUT (DIRECT RF)
PCI BACKPLANE
PCI INTERFACE
303
DOCSIS MAC
310
304
312
ANALOG INPUT (DIRECT RF)
PC
302
DOWNSTREAM INTERFACE
QAM MOD
CMTS IF (TEST)
50 MHz PSCLK
MPEG INTERFACE
CNTL
SATELLITE MODULATOR
204
70 MHz DOWNSTREAM

FIG. 4A

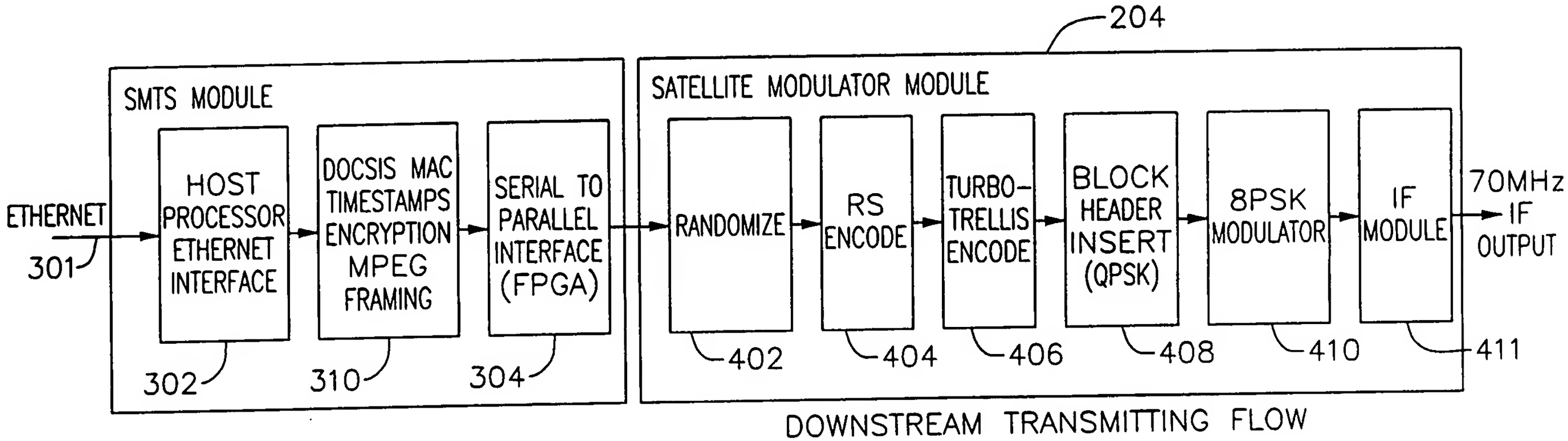

204
SMTS MODULE
SATELLITE MODULATOR MODULE
ETHERNET
301
HOST PROCESSOR ETHERNET INTERFACE
302
DOCSIS MAC TIMESTAMPS ENCRYPTION MPEG FRAMING
310
SERIAL TO PARALLEL INTERFACE (FPGA)
304
RANDOMIZE
402
RS ENCODE
404
TURBO-TRELLIS ENCODE
406
BLOCK HEADER INSERT (QPSK)
408
8PSK MODULATOR
410
IF MODULE
411
70MHz IF OUTPUT
DOWNSTREAM TRANSMITTING FLOW

FIG. 4B

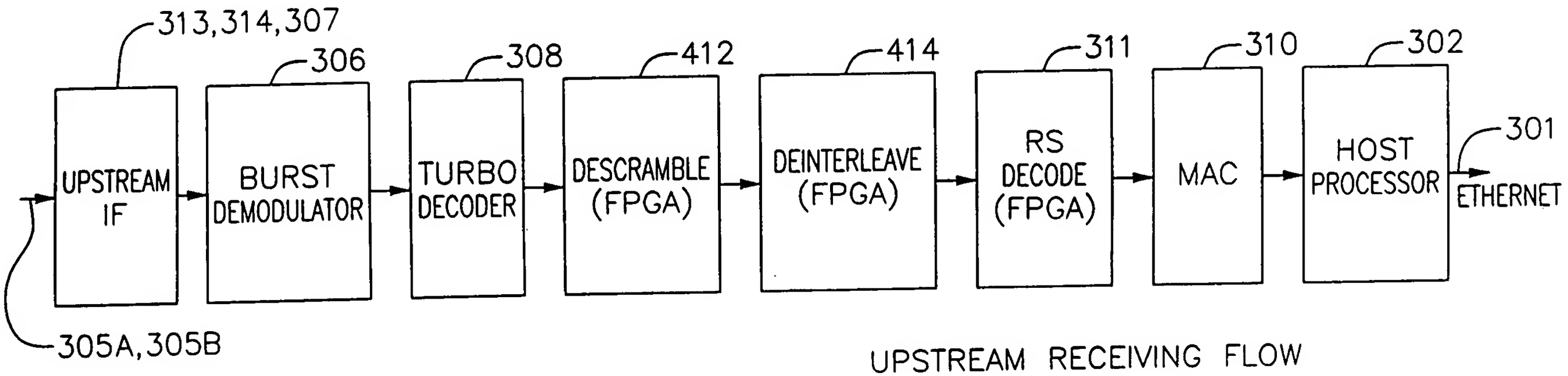
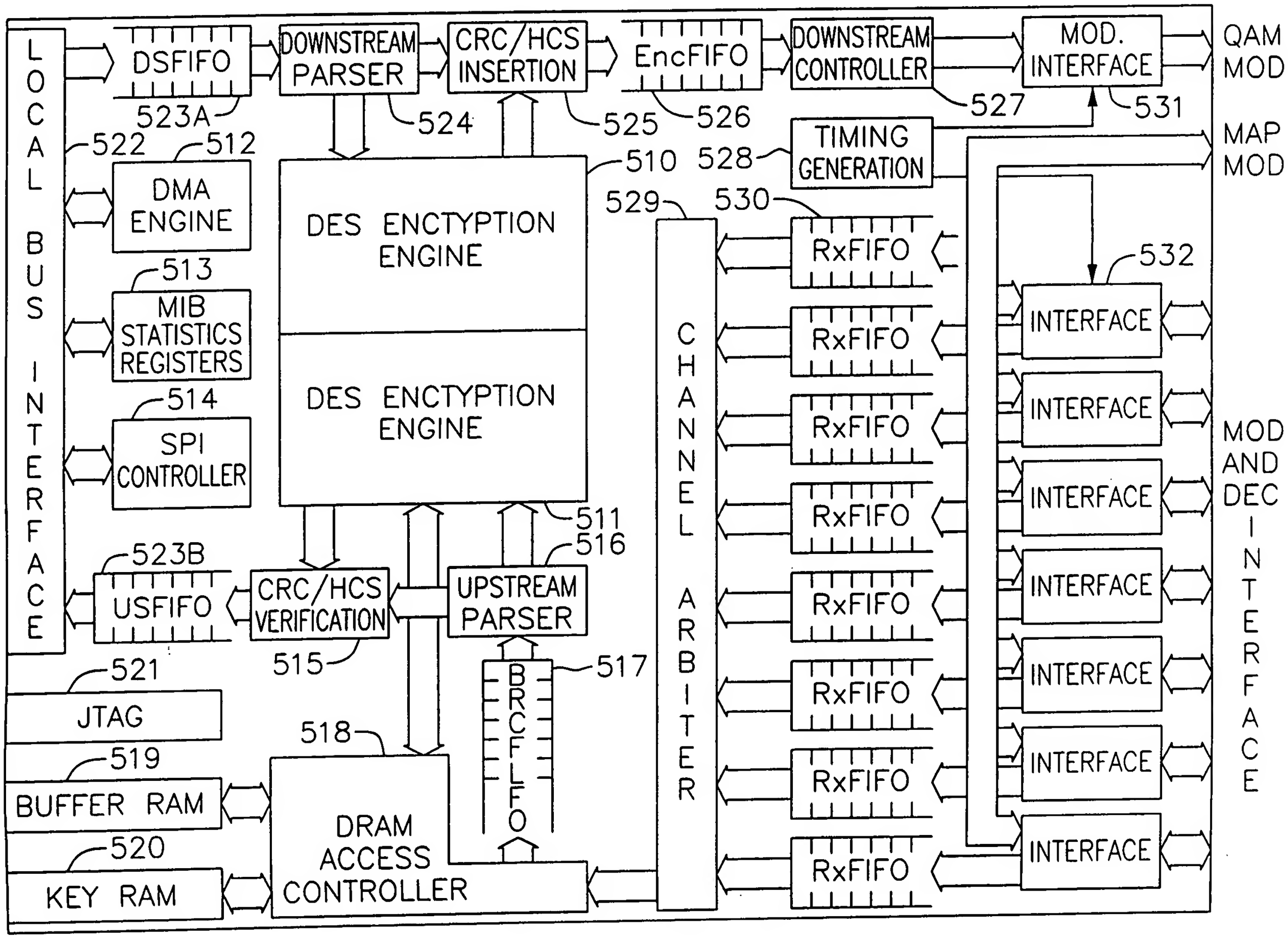

313,314,307
UPSTREAM IF
306
BURST DEMODULATOR
308
TURBO DECODER
412
DESCRAMBLE (FPGA)
414
DEINTERLEAVE (FPGA)
311
RS DECODE (FPGA)
310
MAC
302
HOST PROCESSOR
301
ETHERNET
305A,305B
UPSTREAM RECEIVING FLOW

FIG.5


LOCAL BUS INTERFACE
DSFIFO
523A
DOWNSTREAM PARSER
524
CRC/HCS INSERTION
525
EncFIFO
526
DOWNSTREAM CONTROLLER
527
MOD. INTERFACE
531
QAM MOD
MAP MOD
522
512
DMA ENGINE
513
MIB STATISTICS REGISTERS
514
SPI CONTROLLER
DES ENCTYPTION ENGINE
510
DES ENCTYPTION ENGINE
511
528
TIMING GENERATION
529
530
CHANNEL ARBITER
RxFIFO
RxFIFO
RxFIFO
RxFIFO
RxFIFO
RxFIFO
RxFIFO
532
INTERFACE
INTERFACE
INTERFACE
INTERFACE
INTERFACE
INTERFACE
INTERFACE
MOD AND DEC INTERFACE
523B
USFIFO
CRC/HCS VERIFICATION
515
UPSTREAM PARSER
516
BRCFIFO
517
521
JTAG
518
519
BUFFER RAM
DRAM ACCESS CONTROLLER
520
KEY RAM

II II

FIG. 6

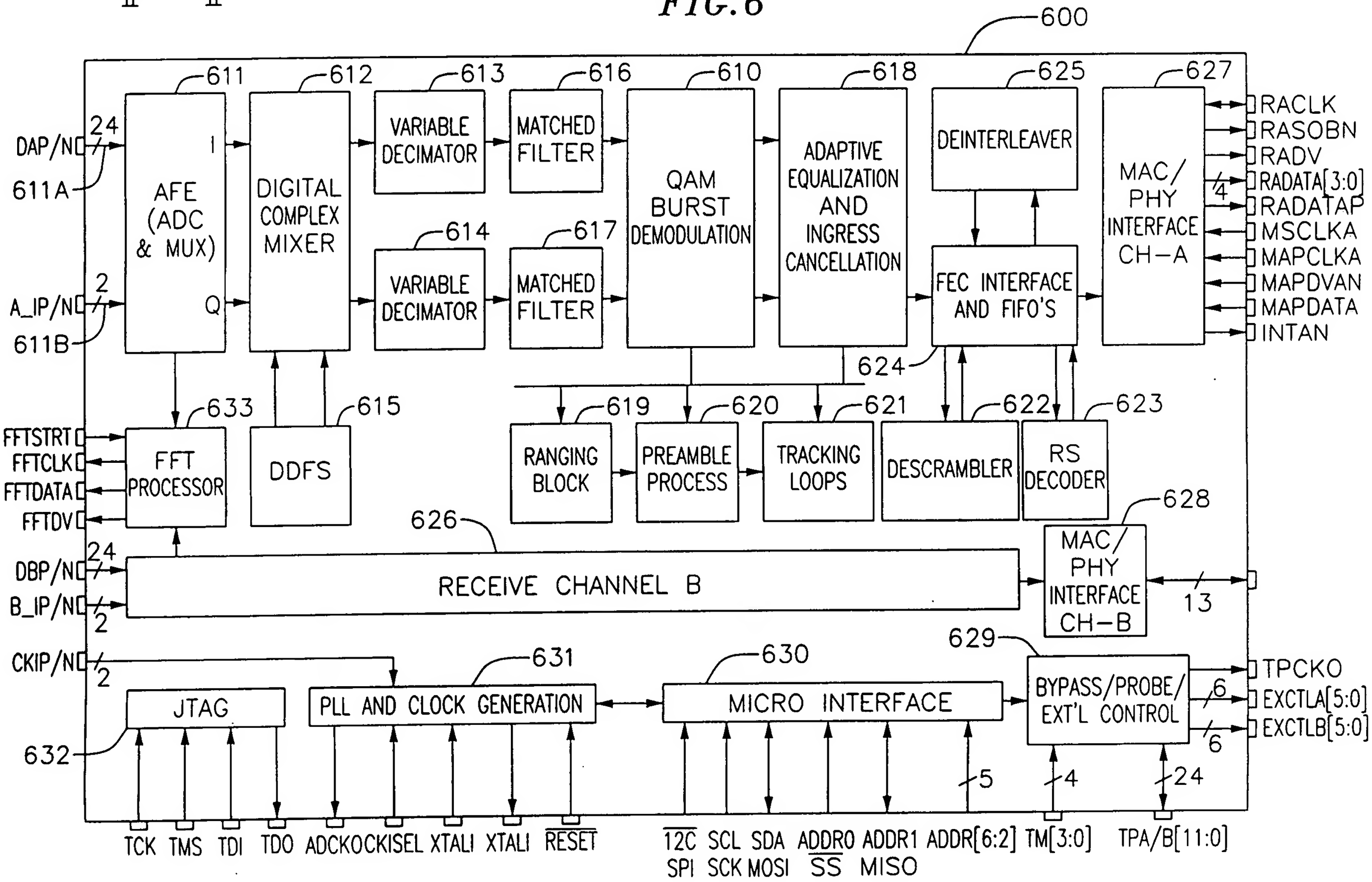

600
611
612
613
616
610
618
625
627
DAP/N
24
611A
AFE (ADC & MUX)
I
Q
DIGITAL COMPLEX MIXER
VARIABLE DECIMATOR
MATCHED FILTER
QAM BURST DEMODULATION
ADAPTIVE EQUALIZATION AND INGRESS CANCELLATION
DEINTERLEAVER
MAC/ PHY INTERFACE CH-A
A_IP/N
2
611B
614
617
VARIABLE DECIMATOR
MATCHED FILTER
624
RACLK
RASOBN
RADV
RADATA[3:0]
4
RADATAP
MSCLKA
MAPCLKA
MAPDVAN
MAPDATA
INTAN
FEC INTERFACE AND FIFO'S
633
615
619
620
621
622
623
FFTSTRT
FFTCLK
FFTDATA
FFTDV
FFT PROCESSOR
DDFS
RANGING BLOCK
PREAMBLE PROCESS
TRACKING LOOPS
DESCRAMBLER
RS DECODER
626
628
DBP/N
24
B_IP/N
2
RECEIVE CHANNEL B
MAC/ PHY INTERFACE CH-B
13
629
CKIP/N
2
631
630
JTAG
PLL AND CLOCK GENERATION
MICRO INTERFACE
BYPASS/PROBE/ EXT'L CONTROL
TPCKO
6
EXCTLA[5:0]
EXCTLB[5:0]
6
632
5
4
24
TCK TMS TDI TDO ADCKO CKISEL XTALI XTALI RESET
I2C SCL SDA ADDR0 ADDR1 ADDR[6:2] TM[3:0] TPA/B[11:0]
SPI SCK MOSI SS MISO

FIG. 7

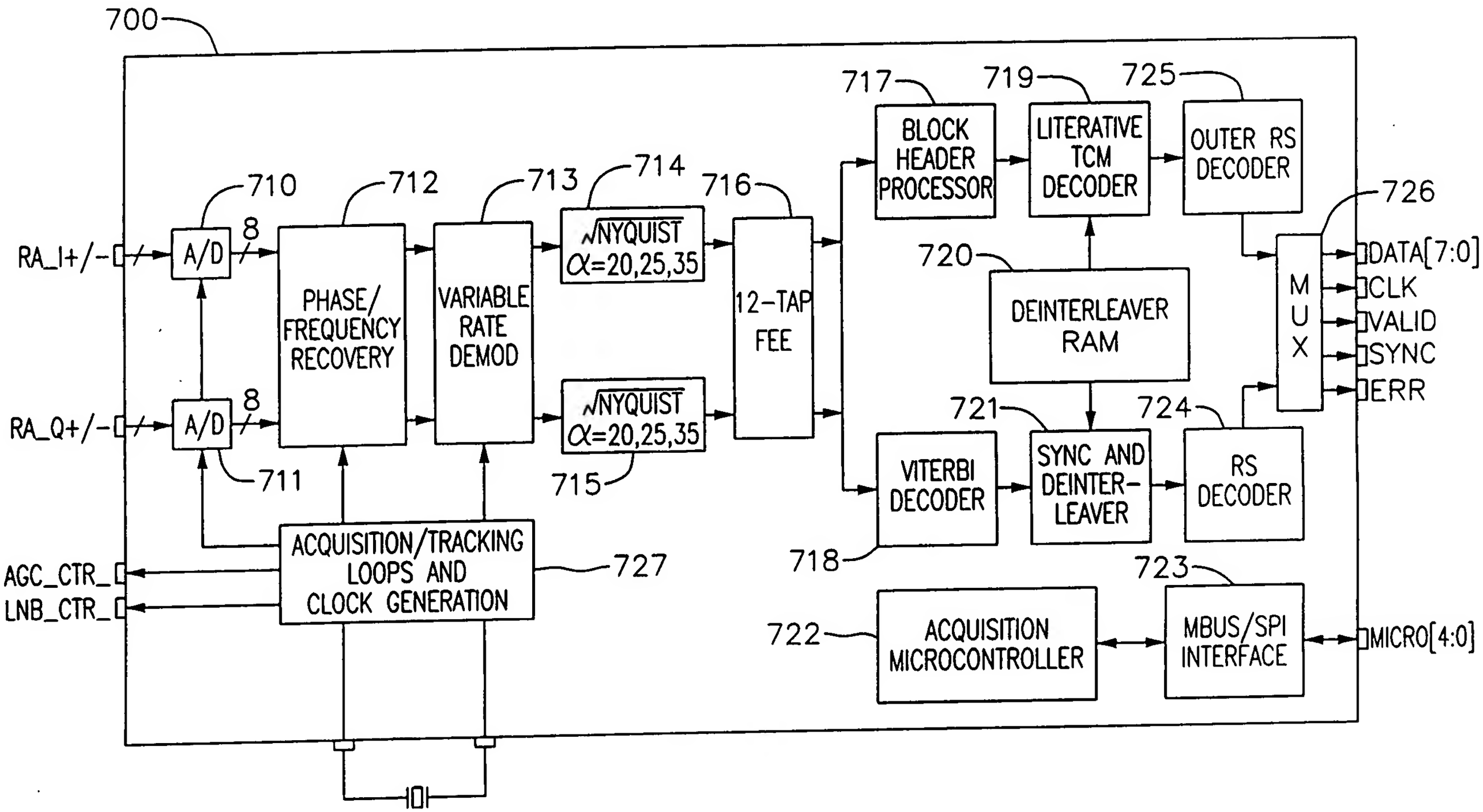

700
717
719
725
BLOCK HEADER PROCESSOR
LITERATIVE TCM DECODER
OUTER RS DECODER
710
712
713
714
716
726
RA_I+/-
A/D
8
PHASE/ FREQUENCY RECOVERY
VARIABLE RATE DEMOD
√NYQUIST α=20,25,35
12-TAP FEE
720
DEINTERLEAVER RAM
M U X
DATA[7:0]
CLK
VALID
SYNC
ERR
RA_Q+/-
A/D
8
711
715
721
724
VITERBI DECODER
SYNC AND DEINTER-LEAVER
RS DECODER
718
ACQUISITION/TRACKING LOOPS AND CLOCK GENERATION
727
AGC_CTR_
LNB_CTR_
723
722
ACQUISITION MICROCONTROLLER
MBUS/SPI INTERFACE
MICRO[4:0]

FIG.8

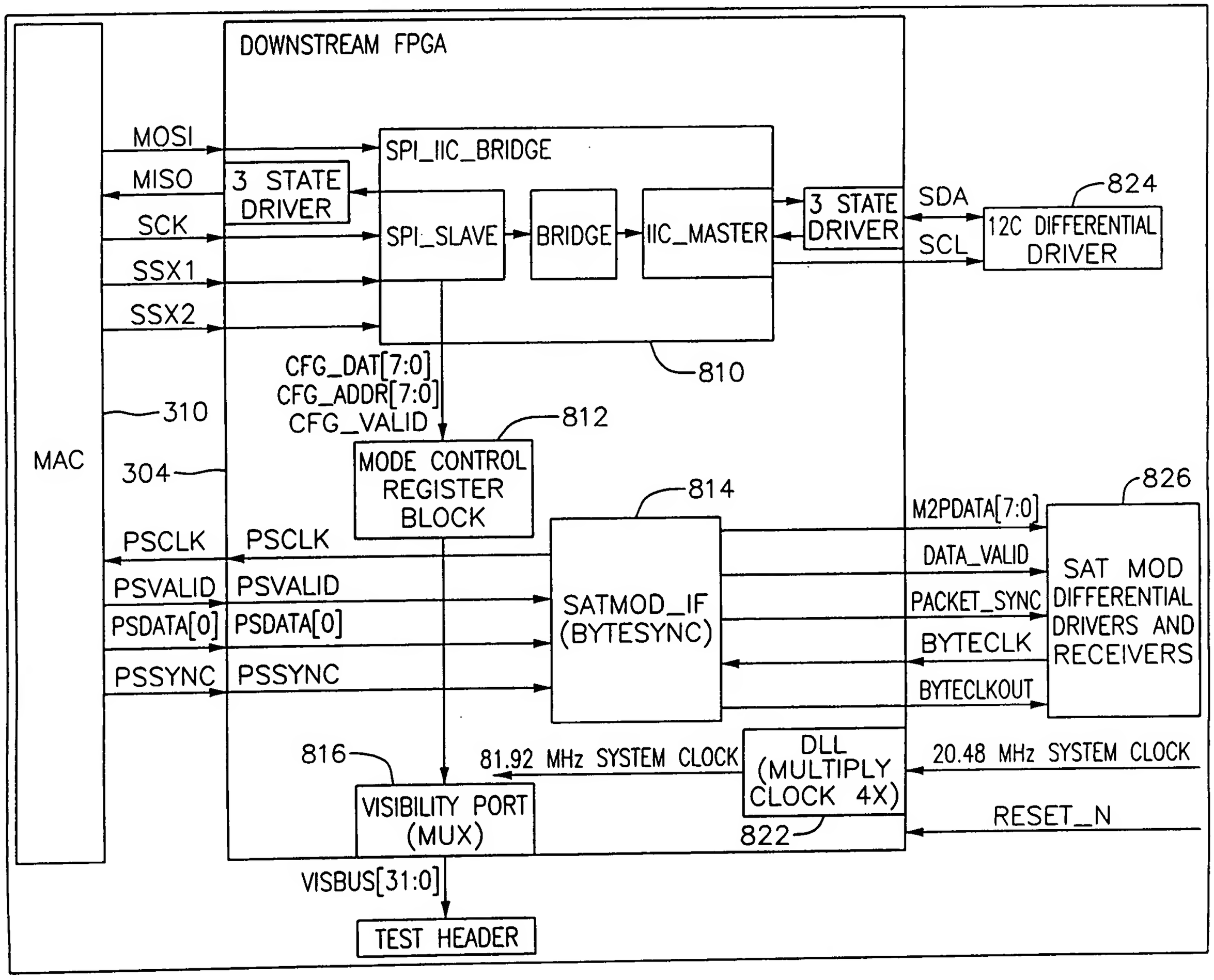

DOWNSTREAM FPGA
MOSI
MISO
SCK
SSX1
SSX2
SPI_IIC_BRIDGE
3 STATE DRIVER
SPI_SLAVE
BRIDGE
IIC_MASTER
3 STATE DRIVER
SDA
SCL
824
12C DIFFERENTIAL DRIVER
810
CFG_DAT[7:0]
CFG_ADDR[7:0]
CFG_VALID
812
310
MAC
304
MODE CONTROL REGISTER BLOCK
814
826
M2PDATA[7:0]
DATA_VALID
PACKET_SYNC
BYTECLK
BYTECLKOUT
SAT MOD DIFFERENTIAL DRIVERS AND RECEIVERS
PSCLK
PSCLK
PSVALID
PSVALID
PSDATA[0]
PSDATA[0]
PSSYNC
PSSYNC
SATMOD_IF (BYTESYNC)
816
81.92 MHz SYSTEM CLOCK
DLL (MULTIPLY CLOCK 4X)
20.48 MHz SYSTEM CLOCK
RESET_N
822
VISIBILITY PORT (MUX)
VISBUS[31:0]
TEST HEADER

FIG. 9

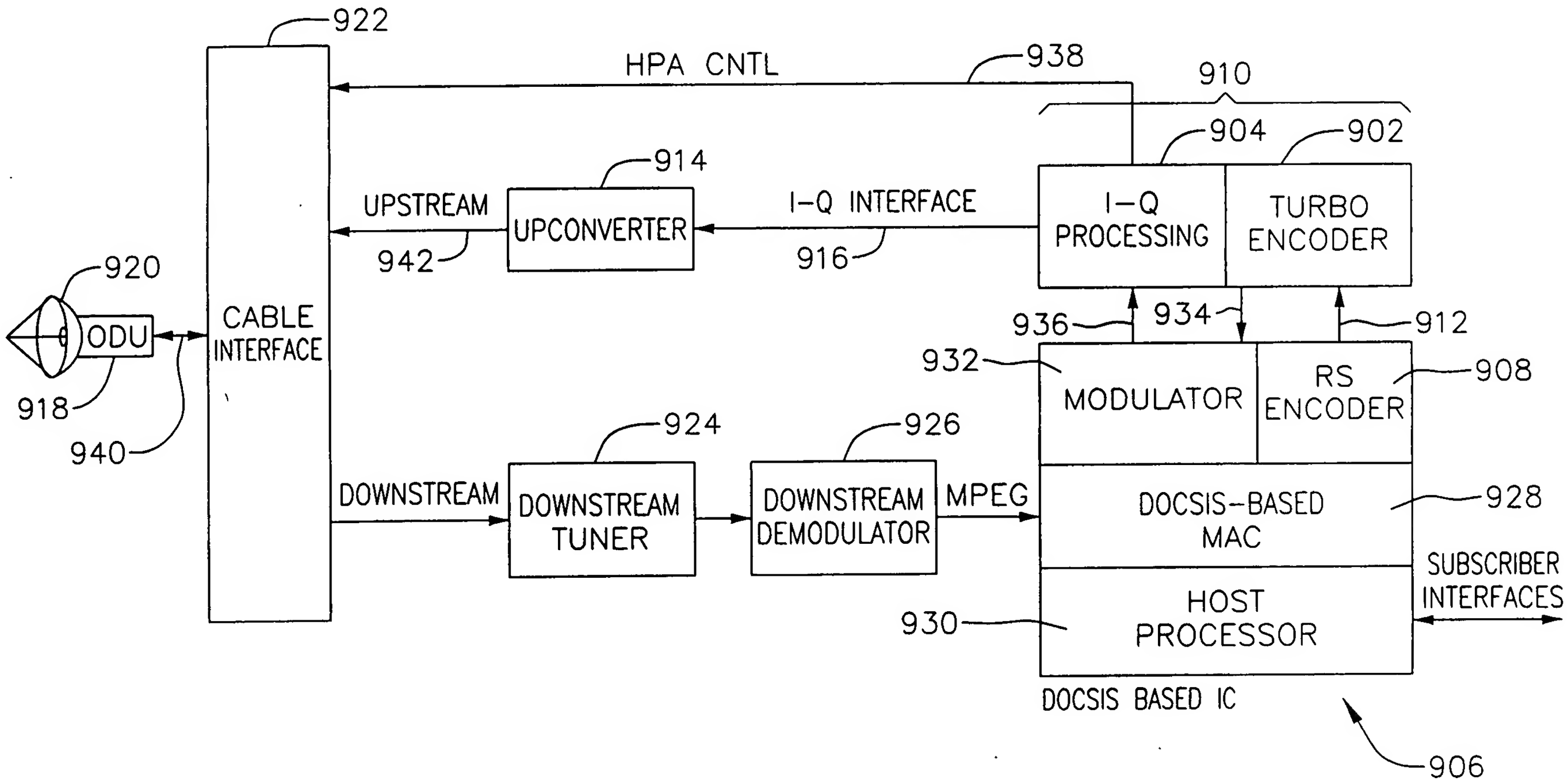
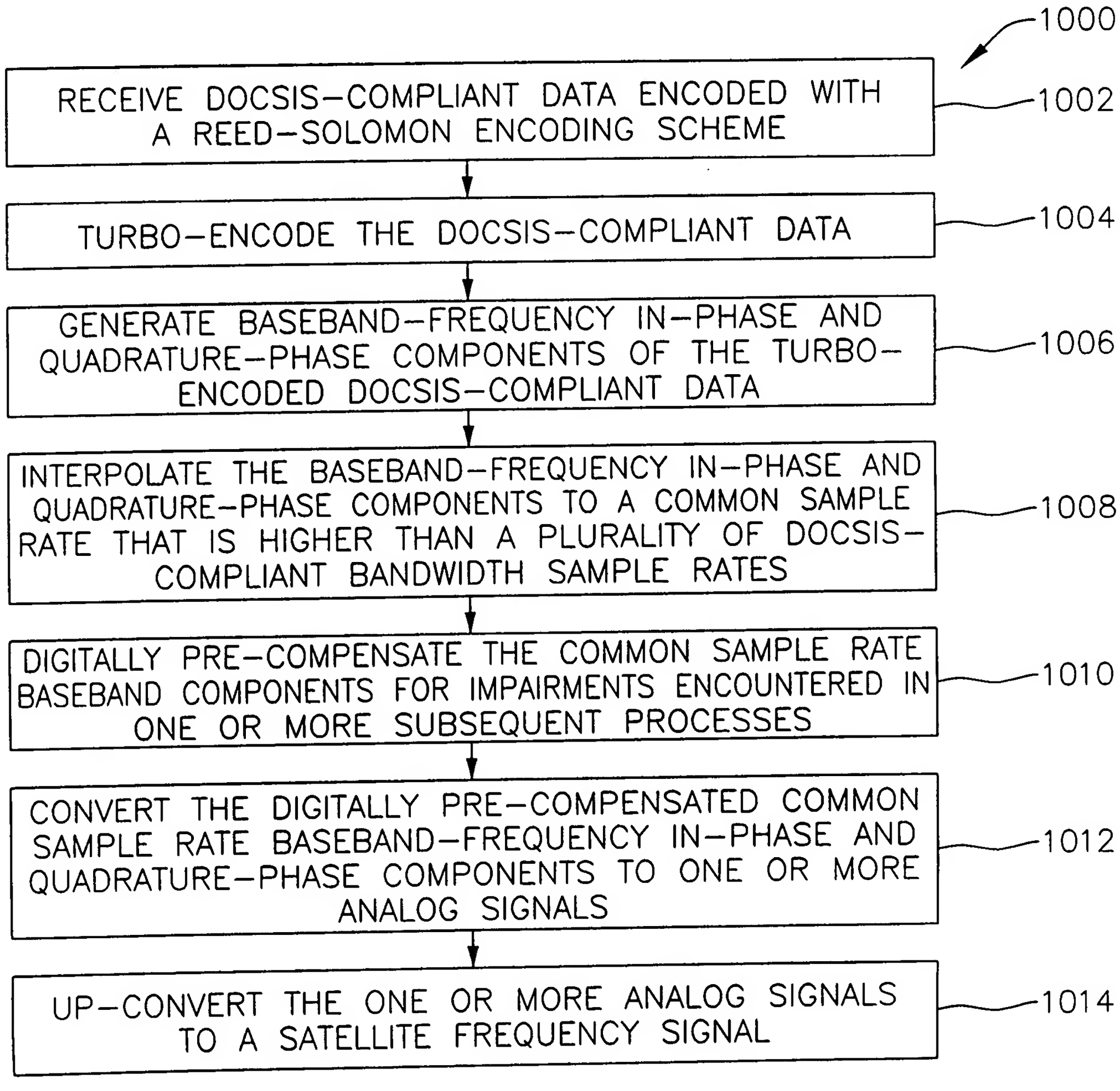

922
HPA CNTL
938
910
904
902
914
UPSTREAM
UPCONVERTER
I-Q INTERFACE
I-Q PROCESSING
TURBO ENCODER
920
942
916
ODU
CABLE INTERFACE
936
934
912
932
MODULATOR
RS ENCODER
908
918
940
924
926
DOWNSTREAM
DOWNSTREAM TUNER
DOWNSTREAM DEMODULATOR
MPEG
DOCSIS-BASED MAC
928
SUBSCRIBER INTERFACES
930
HOST PROCESSOR
DOCSIS BASED IC
906

FIG. 10


1000
RECEIVE DOCSIS-COMPLIANT DATA ENCODED WITH A REED-SOLOMON ENCODING SCHEME
1002
TURBO-ENCODE THE DOCSIS-COMPLIANT DATA
1004
GENERATE BASEBAND-FREQUENCY IN-PHASE AND QUADRATURE-PHASE COMPONENTS OF THE TURBO-ENCODED DOCSIS-COMPLIANT DATA
1006
INTERPOLATE THE BASEBAND-FREQUENCY IN-PHASE AND QUADRATURE-PHASE COMPONENTS TO A COMMON SAMPLE RATE THAT IS HIGHER THAN A PLURALITY OF DOCSIS-COMPLIANT BANDWIDTH SAMPLE RATES
1008
DIGITALLY PRE-COMPENSATE THE COMMON SAMPLE RATE BASEBAND COMPONENTS FOR IMPAIRMENTS ENCOUNTERED IN ONE OR MORE SUBSEQUENT PROCESSES
1010
CONVERT THE DIGITALLY PRE-COMPENSATED COMMON SAMPLE RATE BASEBAND-FREQUENCY IN-PHASE AND QUADRATURE-PHASE COMPONENTS TO ONE OR MORE ANALOG SIGNALS
1012
UP-CONVERT THE ONE OR MORE ANALOG SIGNALS TO A SATELLITE FREQUENCY SIGNAL
1014

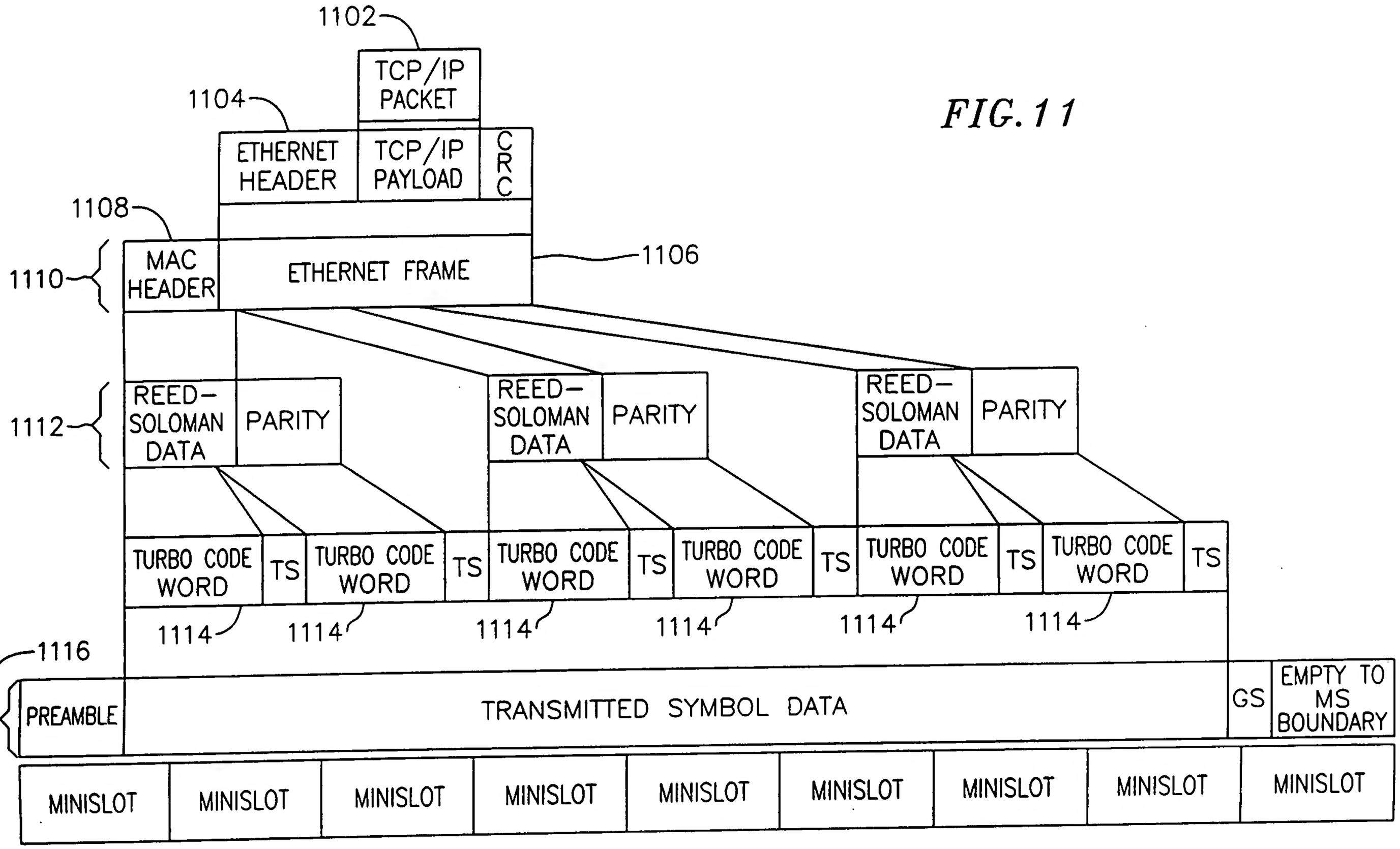

1102
TCP/IP PACKET
1104
ETHERNET HEADER
TCP/IP PAYLOAD
CRC
1108
1110
MAC HEADER
ETHERNET FRAME
1106
1112
REED-SOLOMAN DATA
PARITY
REED-SOLOMAN DATA
PARITY
REED-SOLOMAN DATA
PARITY
TURBO CODE WORD
TS
TURBO CODE WORD
TS
TURBO CODE WORD
TS
TURBO CODE WORD
TS
TURBO CODE WORD
TS
TURBO CODE WORD
TS
1114
1114
1114
1114
1114
1114
1116
PREAMBLE
TRANSMITTED SYMBOL DATA
GS
EMPTY TO MS BOUNDARY
MINISLOT
MINISLOT
MINISLOT
MINISLOT
MINISLOT
MINISLOT
MINISLOT
MINISLOT
MINISLOT

FIG. 11

FIG. 12

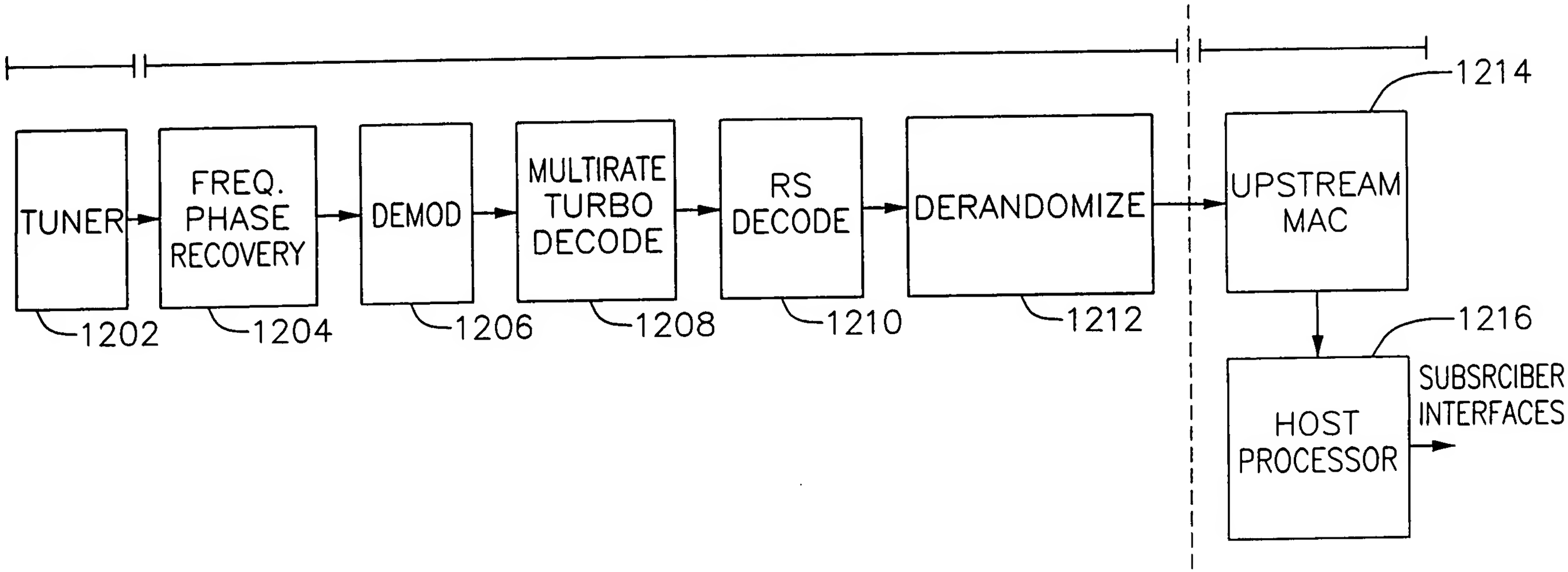

TUNER
FREQ. PHASE RECOVERY
DEMOD
MULTIRATE TURBO DECODE
RS DECODE
DERANDOMIZE
UPSTREAM MAC
HOST PROCESSOR
SUBSRCIBER INTERFACES
1202
1204
1206
1208
1210
1212
1214
1216

FIG. 13

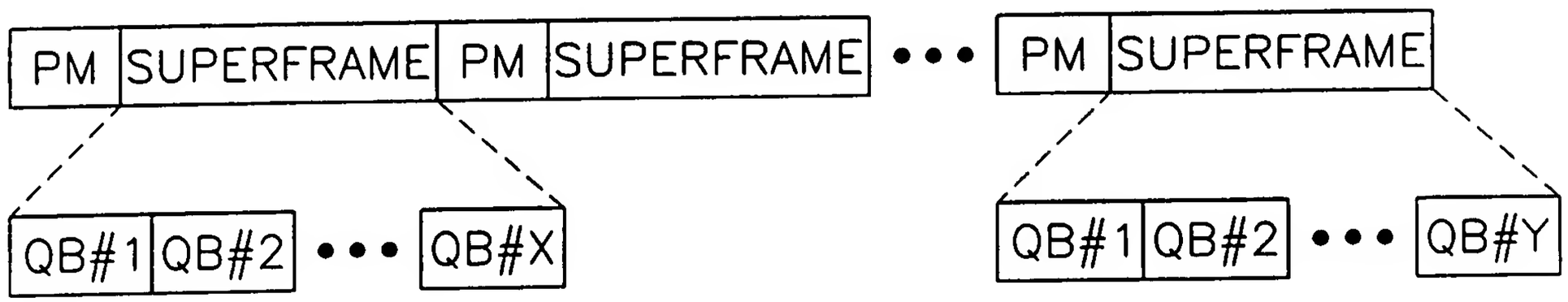
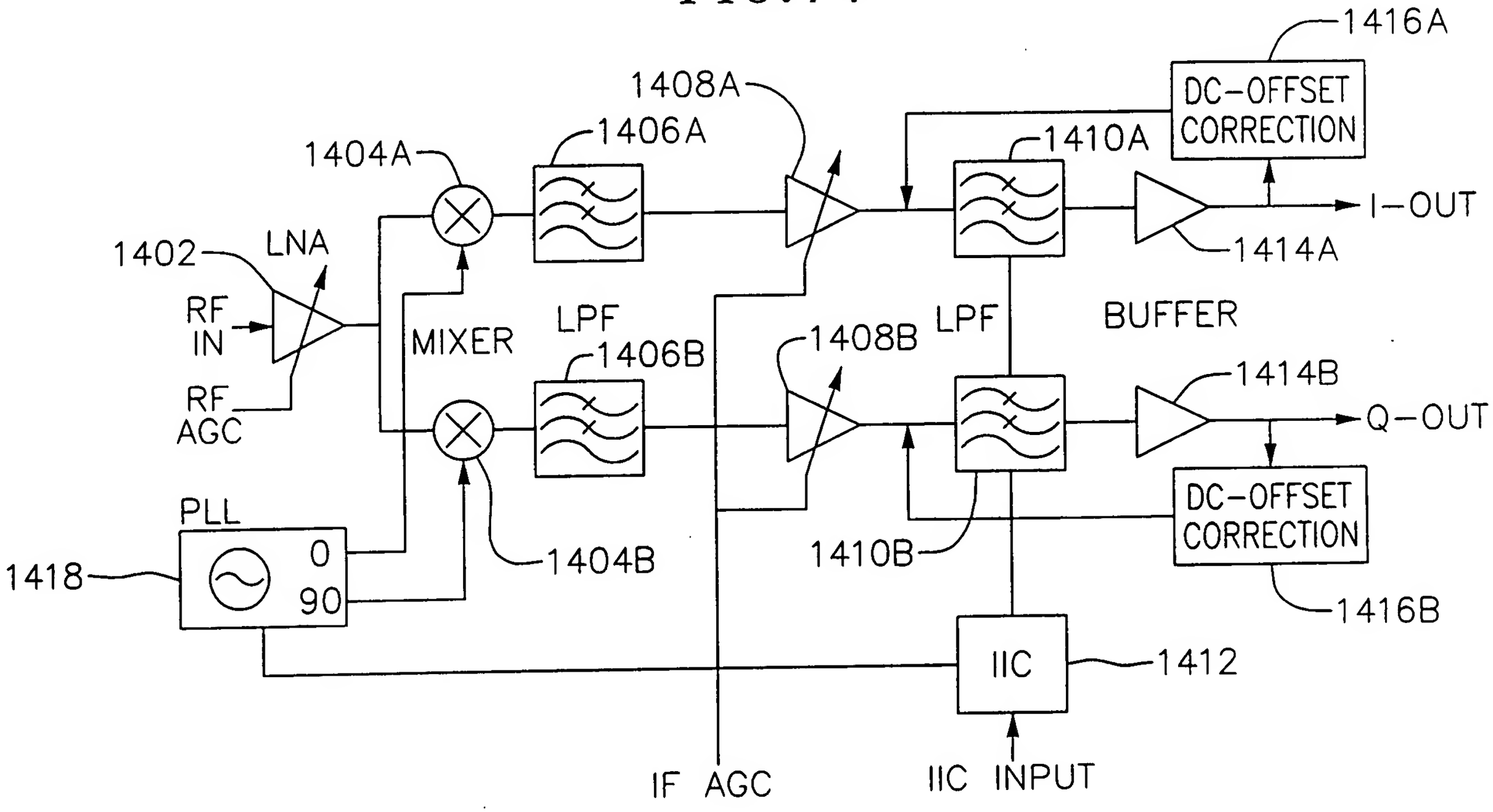

PM
SUPERFRAME
PM
SUPERFRAME
PM
SUPERFRAME
QB#1
QB#2
QB#X
QB#1
QB#2
QB#Y

FIG. 14


1416A
DC-OFFSET CORRECTION
1408A
1406A
1410A
1404A
I-OUT
1414A
1402
LNA
RF IN
RF AGC
MIXER
LPF
1406B
1408B
LPF
BUFFER
1414B
Q-OUT
DC-OFFSET CORRECTION
1416B
PLL
0
90
1418
1404B
1410B
IIC
1412
IF AGC
IIC INPUT